REMARKS

Claims 1-23 remain active in this application. Claims 21 - 23 have been withdrawn from consideration in response to a requirement for restriction and an election without traverse as noted in the present office action; the election without traverse being hereby confirmed. New claim 24 has been added to more fully claim the subject matter regarded to be the invention. By this amendment, claims 1, 6, 7, 9, 12 - 20 and withdrawn claim 22 are amended to improve form; largely adopting the Examiner's suggestions. The foregoing separate sheets marked as "Listing of Claims" show all the claims in the application, with an indication of the current status of each. The amendments made above are not believed to be substantive and no new matter has been introduced into the application thereby. The indication of allowability of the subject matter of claims 2 - 6 and 13 - 17 is noted with appreciation.

Drawings

The Examiner has objected to the drawings due to non-uniformity of lines and/or letters in Figures 5c and 6a. Applicant herewith submits replacement sheets of corrected drawings for Figures 5c and 6a in which all lines and numbers are uniform. No substantive changes have been requested.

In view of the foregoing, Applicant respectfully requests withdrawal of this objection.

Claim Objections

Claim 1 is objected to as lacking the recitation of "using said quantified characteristics" after "domains" in the last line of the claims. Claim 1 has hereby been amended to recite "using said quantified characteristics" after "domain" in the last line of claim 1 as required by the Examiner. Applicant respectfully requests entry of this amendment and withdrawal of this objection.

Claims 5-9, 16 and 20 are objected to due to incorrect antecedent basis, reciting "the" rather than "a". Claims 5-7, 9, 16 and 20 have hereby been amended to recite "a" rather than "the" where appropriate, thereby providing correct antecedent basis. However, claim 8 has not

been amended. Applicant respectfully submits that Examiner has erred in objecting to claim 8; claim 8 does not recite "the step" and thus cannot be deficient in antecedent basis for a step. Further, Examiner has required correction of "the substrate" to "a substrate" in claims 5 and 9. However, this recitation occurs in claim 5 and 16 (not 9). Claims 5 and 16 have thus been amended to recite "a" rather than "the" substrate. Applicant respectfully requests entry of the amendments to claims 5-7, 9, 16 and 20 and withdrawal of this objection.

Claim 12 is objected to as lacking the recitation of "using said quantified characteristics" after "unit cell" in line 19. Claim 12 has hereby been amended to recite "using said quantified characteristics" after "unit cell" in line 19 as required by the Examiner. Applicant respectfully requests entry of this amendment and withdrawal of this objection.

Claims 14 and 15 are objected to due to the recitation of "claim 11" instead of "claim 13, thereby lacking proper antecedent basis. Claims 14 and 15 have hereby been amended to recite dependency from claim 13, thereby providing proper antecedent basis. Applicant respectfully requests entry of this amendment and withdrawal of this objection.

Claim 19 is objected to due to the recitation of "claims 10" rather than "claim 12", thereby lacking proper antecedent basis. Claim 19 has hereby been amended to recite "claim 12", thereby providing proper antecedent basis. Applicant respectfully requests entry of this amendment and withdrawal of this objection.

Claims 2-11 and 13-20 are objected to as incorporating these same errors by dependency. Claims 2-11 and 13-20 have hereby been amended to correct these errors as follows: claims 13 and 16-20 have been amended to change "the" to "a" to provide correct antecedent basis, and to recite dependency from claim 12, rather than from claim 10. Applicant respectfully requests withdrawal of this objection.

Claim Rejections: 35 USC § 101

Claims 1-20 stand rejected under 35 USC § 101 as unpatentable due to, in the opinion of the Examiner, lacking practical application.

The Examiner has suggested that a suitable practical application might be "determining latchup or noise or defect" or "re-designing the circuit based on the total minor carrier transmission evaluated".

Claims 1 is hereby amended to recite an additional step of determining latchup or noise or defect in said semiconductor chip design based on results of said evaluating step. In addition, new claim 24 has been presented in which an additional step of redesigning said chip to avoid latchup or noise or defect determined in said determining step is added to the method. Support for this amendment and this new claim is found, for example, on page 10 in paragraph 40, where the prediction of noise and latchup using the method are described, as is the development of designs that avoid noise and latchup.

It is also respectfully submitted that the claims, as rejected, are manifestly statutory subject matter. The subject matter of the invention as originally claimed clearly has utility in quantitatively evaluating semiconductor device designs for locations where conditions conducive to latchup (or generation of noise even if latchup does not occur) may be likely. In this sense the invention is analogous to a simulator device or method which manifestly has utility and practical application and thus is manifestly statutory subject matter. Nevertheless, since the Examiner's suggestion for amendment to avoid this ground of rejection has been adopted, it is clear that the claims now recite subject matter which is even more manifestly statutory subject matter.

In view of he foregoing, Applicant requests reconsideration of claims 1-20 and withdrawal of this ground of rejection.

Claim Rejections: 35 USC § 103(a)

Claims 1, 7 - 8, 10 - 12 and 18 - 19 have been rejected under 35 U.S.C. §103 as being unpatentable over Nagase et al. in view of Finman. claims 9 and 20 have been rejected under 35 U.S.C. §103 as being unpatentable over Nagase et al. in view of Finman and the Krieger article. Both of these grounds of rejection are respectfully traversed.

The invention is directed to a method and apparatus for analysis of semiconductor device designs for locations where latchup (or generation of noise even if latchup does not occur - see paragraph 9, last sentence) can occur. Paragraphs 6 and 7 of the specification indicates that

latchup typically occurs where there are structures which form a pnpn structure that can function as two bipolar transistors having the bases and collectors cross-coupled to provide regenerative feedback and is a function of bipolar current gain of the transistors, substrate resistance and spacings, well resistance and spacings and isolation regions and that likelihood of or sensitivity to latchup to excess minority carriers is also a function of these structures and their spacings. The invention thus fundamentally provides an analysis of locations where excess carriers are likely to occur by analyzing regions or domains of a structure including a structure or "shape" presenting a boundary or gradient for probability of transmission of carriers and probability of reflection and/or absorption of carriers (e.g. by recombination), which are subtractions from transmissions, along an arc (representing a conduction path) intersecting a shape, all of which either add to of subtract from the probability of collection of excess carriers at a given location or within a given region along the arc.

It is respectfully submitted that Nagase et al. has very little, if anything, to do with the present invention and is substantially non-analogous thereto. While Nagase et al. is directed to analysis of currents in order to evaluate radiated magnetic fields, the currents being evaluated in Nagase et al. are almost certain to be orders of magnitude greater than those to which the present invention is directed and, more importantly, are necessarily currents which are *net of any absorption* (e.g. a subtraction from current) or at least where absorption and reflection are negligible, rather than analysis of the probability of accumulation of carriers or impediments to reduction of carrier populations (diametrically opposed to the analysis of currents of Nagase et al.). Moreover, it is assumed in Nagase et al. that the body of material in which currents are analyzed is more or less homogeneous metal, as distinct from "a semiconductor chip design using shapes", as claimed, and it is the *mutual impedance* between divided metal parts which is analyzed to derive the currents in the respective parts of the metal in accordance with the "moment method" (summarized at column 2, lines 10 - 30) rather than the transmission, absorption and reflection within a single domain, as claimed. Even more importantly, Nagase et al. is fundamentally directed to the problem of forming an intelligible display from data obtained using a known "moment method" technique of analysis since the "moment method" may not provide regularly spaced division of the metal body and may include disproportionately sized

parts of the metal body being analyzed and therefore the currents in respective parts of the metal body are not necessarily of the same scale (see, for example, column 2, lines 44 - 49, and the summary of the solution provided by Nagase et al at column 8, lines 16 - 21). Nagase et al. thus appears to merely map the currents derived using the known "moment method" of analysis onto a regularly spaced grid so that the indicia representing currents can be displayed in a manner which is intelligible to an observer. Therefore, but for the use of a grid for reference in scaling of currents which are derived by the "moment method", Nagase et al has virtually nothing in common with the present invention and the use of the grid, the factors affecting current, the magnitude of the current and the goal of the analysis, the calculation (in the moment method) of mutual impedance between parts (rather than the analysis of each domain), the definition of parts (without reference to shapes or an arc by which domains are defined, as claimed), the analysis of a metal (as opposed to semiconductor) body of arbitrary shape but without internal shapes in accordance with the moment method, determination of current magnitude (rather than probability of carrier accumulation) and the like and even the scale of the body being analyzed and the magnitude of the phenomena contributing to the effects for which analysis is desired are all diametrically opposed to and teach away from the invention.

The Examiner admits the fundamental difference from Nagase et al. from the claimed invention in that Nagase et al. does not consider effects of absorption or reflection within or at boundaries of domains (although failing to appreciate the implications thereof, as discussed above) and cites Finman for disclosure of consideration thereof, citing column 7, line 15, to column 8, line 31. However, it is respectfully submitted that Finman is also largely non-analogous to the present invention. The circuit being described in the passage of Finman relied upon by the examiner is an equivalent circuit of a PIN diode *circuit* which functions as an "RF or other electromagnetic signal attenuator/detector" (column 7, lines 1 - 2) rather than "a semiconductor chip design using shapes". Moreover, Finman does not define an arc crossing those shapes or "domains in relation to points on said arc", as claimed. Further, the "reflection, transmission and absorption coefficients appear to refer to those parameters in regard to a signal and not to carriers (e.g. charge). Therefore, aside from using the terms "reflection transmission and absorption" in an altogether different context and in regard to an altogether different type of

quantity (e.g. a signal rather than a carrier in a semiconductor), Finman has no discernable relevance to the present invention. Moreover, it is respectfully submitted that Finman contains no motivation for combination with Nagase et al., particularly to provide enhanced accuracy as the Examiner asserts since, as noted above, the effects of interest in Nagase et al. are electromagnetic fields caused by net currents in a metal body of a *circuit component* and reflection, transmission and absorption of signals in a *circuit*, while possibly relevant to current and voltage *magnitude* at various nodes of the circuit, are not disclosed, in either Nagase et al. or Finman, to affect current distribution in any given component, much less the probability of carrier accumulation as in the present invention.

Therefore, it is respectfully submitted that the proposed combination of teachings of Nagase et al. and Finman is improper and, in any case, both references are substantively irrelevant to the present invention, as claimed and, moreover, do not answer numerous explicit recitations of the claims as well as being non-analogous thereto and lacking motivation for their proposed combination. Accordingly, it is respectfully submitted that the Examiner has failed to make a *prima facie* demonstration of obviousness of any of claims 1, 7 - 8, 10 - 12 or 18 - 19 and the ground of rejection based on Nagase et al. and Finman is clearly in error and untenable. Accordingly, reconsideration and withdrawal of the same are respectfully requested.

In regard to claims 9 and 20, the Examiner admits that the combination of Nagase et al. and Finman does not relate to a pnpn structure (although this glosses the fact, argued above, that neither is at all concerned with latchup or noise which typically occurs in a pnpn structure) and cites the Krieger article for such teaching. While Krieger involves latchup and pnpn structures, as is the invention, it is non-analogous to Nagase et al. and Finman and is not properly combinable therewith for that reason; having no discernible utility therein and lacking disclosed motivation for the combination. Further, it does not mitigate any of the numerous and fundamental deficiencies of the combination of Nagase et al. and Finman as discussed above and the Examiner has not asserted that it does. While Krieger discusses a bipolar transistor analysis in regard to latchup, that analysis does not appear to bear any relevance to the analysis method or apparatus claimed and, again, the Examiner has not asserted that it does. Therefore, it is respectfully submitted that the combination of Nagase et al., Finman and Krieger, even if

(*arguendo*) proper, does not answer the recitations of the claims or provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness for the simple reason that the combination of teachings does not lead to an expectation of success in providing a systematic and flexible method or apparatus for estimating the probability of conditions which could cause latchup or generation of noise, much less the particularly straightforward analysis claimed which can be readily automated. Therefore, it is respectfully submitted that the rejection of claims 9 and 20 is also clearly in error and, upon reconsideration, should be withdrawn.

Concluding remarks

In view of the foregoing, it is requested that the application be reconsidered, that claims 1 - 20 and 24 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: ruth@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to International Business Machines Deposit Account No. 09-0456.

Respectfully submitted,

Ruth E. Tyler-Cross
Reg. No. 45,922

Whitham, Curtis, Christofferson & Cook, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
703-787-9400 (Telephone)
703-787-7557 (Facsimile)